WHAT IS CLAIMED IS:

1. A method for adjusting input clock timing affecting performance of data input operations of an integrated circuit comprising the steps of:

successive testing data input operation with an incrementally delayed input clock until all input operations pass;

determining target state programming bits to set the least input clock delay passing the input operation test;

writing the target state of programming bits into a write once memory; and

controlling input clock delay corresponding to said programming bits stored in the write once memory.

2. The method of claim 1, further comprising:

after determining the target state programming bits and before writing the target state programming bits into the write once memory

storing the target state programming bits in a read/write memory,

testing a non-memory portion of integrated circuit while controlling input delay clock corresponding to the target state programming bits stored in the read/write memory,

determining if the non-memory portion fails the test, and

incrementally delaying the input clock and repeating said steps of storing, testing and determining until the non-memory portion passes the test.

3. The method of claim 1 wherein:

said step of writing the target state of programming bits into the write once memory includes

applying a programming voltage to each programming bit whose target state is a first digital state,

determining whether each programming bit whose target state is the first digital state reads as the first digital state, and

applying the programming voltage to each programming bit whose target state is the first digital state but which reads a second, opposite digital state,

repeating said steps of determining and applying the programming voltage to each programming bit whose target state is the first digital state but which reads the second digital state until all programming bits whose target state is the first digital state read as the first digital state.

4. The method of claim 1 wherein:

said step of writing the target state of programming bits into a write once memory includes writing programming bits not related to data input operations performance.

5. The method of claim 4 wherein:

the programming bits not related to data input operations performance include an identification code of a specific die.

6. The method of claim 1 further comprising the steps of:

successive testing data output operation with an incrementally delayed output clock until all output operations pass;

determining output target state programming bits to set the least output clock delay passing the output operation test;

writing the output target state of programming bits into the write once memory; and

controlling output clock delay corresponding to said programming bits stored in the write once memory.

7. A method for adjusting output clock timing affecting performance of data output operations of an integrated circuit comprising the steps of:

successive testing data output operation with an incrementally delayed output clock until all output operations pass;

determining target state programming bits to set the least output clock delay passing the output operation test;

writing the target state of programming bits into a write once memory; and

controlling output clock delay corresponding to said programming bits stored in the write once memory.

8. The method of claim 7, further comprising:

after determining the target state programming bits and before writing the target state programming bits into the write once memory

storing the target state programming bits in a read/write memory,

testing a non-memory portion of integrated circuit while controlling output clock delay corresponding to the target state programming bits stored in the read/write memory, determining if the non-memory portion fails the test, and

incrementally delaying the output clock and repeating said steps of storing, testing and determining until the non-memory portion passes the test.

9. The method of claim 7 wherein:

said step of writing the target state of programming bits into the write once memory includes

applying a programming voltage to each programming bit whose target state is a first digital state,

determining whether each programming bit whose target state is the first digital state reads as the first digital state, and

applying the programming voltage to each programming bit whose target state is the first digital state but which reads a second, opposite digital state,

repeating said steps of determining and applying the programming voltage to each programming bit whose target state is the first digital state but which reads the second digital state until all programming bits whose target state is the first digital state read as the first digital state.

10. The method of claim 7 wherein:

said step of writing the target state of programming bits into a write once memory includes writing programming bits not related to data input operations performance.

11. The method of claim 10 wherein:

the programming bits not related to data input operations performance include an identification code of a specific die.

12. An integrated circuit comprising:

an input terminal for receiving an input signal;

an input register having an input connected to said input terminal, a clock input and an output supplying input data to said integrated circuit, said input register sampling and storing data received at said input upon receipt of a clock pulse at said clock input;

a clock distribution spine for distribution of a clock signal, said clock signal having repetitive clock pulses;

a write once memory having a at least one input delay bit, each input delay bit having an unprogrammed digital state and capable of being changed once to a programmed digital state; and

an input clock delay element having an input receiving said clock signal from said clock distribution spine, a control input receiving said at least one input delay bit and an output connected to said clock input of said input register, said input clock delay element delaying said clock signal an amount corresponding to said digital state of said at least one input delay bit.

13. The integrated circuit of claim 12, further comprising:

an input buffer having an input connected to said input terminal and an output connected to said input of said input register.

14. The integrated circuit of claim 12, wherein:

said input clock delay element includes

a plurality of delay paths, each delay path having an input connected to said clock distribution spine, an output and a unique delay amount; and

a multiplexer having a plurality of inputs, one connected to said output of a corresponding delay path, an output connected to said clock input of said input register and a control input receiving said at least one input delay bit, said multiplexer selecting at said output one of said plurality of inputs corresponding to said at least one input delay bit.

15. The integrated circuit of claim 14, wherein:

each delay path of said clock delay element includes a plurality of inverters having a number corresponding to said unique delay amount.

16. The integrated circuit of claim 12, further comprising:

an output terminal;

an output register having an input receiving outgoing data from said integrated circuit, a clock input and an output connected to said output terminal, said output register sampling and storing data received at said input upon receipt of a clock pulse at said clock input;

said write once memory further having a at least one output delay bit, each output delay bit having an unprogrammed digital state and capable of being changed once to a programmed digital state; and

an output clock delay element having an input receiving said clock signal from said clock distribution spine, a control input receiving said at least one output delay bit and an output connected to said clock input of said output register, said output clock delay element delaying said clock signal an amount corresponding to said digital state of said at least one output delay bit.

17. The integrated circuit of output circuit comprising:

an output terminal;

an output register having an input receiving outgoing data from said integrated circuit, a clock input and an output connected to said output terminal, said output register sampling and storing data received at said input upon receipt of a clock pulse at said clock input;

said write once memory further having a at least one output delay bit, each output delay bit having an unprogrammed digital state and capable of being changed once to a programmed digital state; and

a clock distribution spine for distribution of a clock signal, said clock signal having repetitive clock pulses;

an output clock delay element having an input receiving said clock signal from said clock distribution spine, a control input receiving said at least one output delay bit and an output connected to said clock input of said output register, said output clock delay element delaying said clock signal an amount corresponding to said digital state of said at least one output delay bit.

18. The integrated circuit of claim 17, further comprising:

an output buffer having an input connected to said output terminal of said output register and an output connected to said output terminal.

19. The integrated circuit of claim 17, wherein:

said output clock delay element includes

a plurality of delay paths, each delay path having an input connected to said clock distribution spine, an output and a unique delay amount; and

a multiplexer having a plurality of inputs, one connected to said output of a corresponding delay path, an output connected to said clock input of said input register and a control input receiving said at least one output delay bit, said multiplexer selecting at said output one of said plurality of inputs corresponding to said at least one input delay bit.

20. The integrated circuit of claim 19, wherein:

each delay path of said clock delay element includes a plurality of inverters having a number corresponding to said unique delay amount.